ECE 321

Term Project

2-1 Multiplexer

Brian Becker

Jeremy McConaha

Anthony Mancuso

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# INTRODUCTION

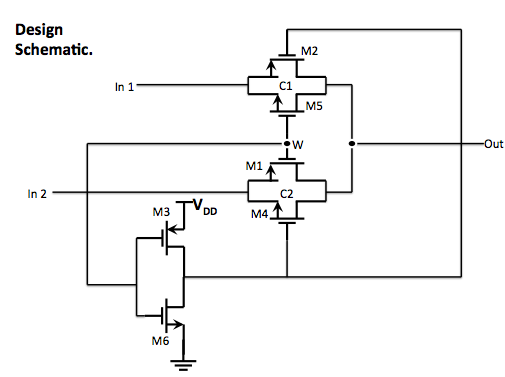
The ECE 321 Fall 2012 2-1 multiplexer project is intended to provide students with exposure to and hands-on practice in design, manufacturing-layout, PSPICE implementation, and analysis of a semiconductor circuit. Design of the circuit will be accomplished in LEDIT using MOSIS 2 µm Process (SCMOS) technology, and the LEDIT layout will be extracted to a PSPICE file for implementation and characterization. Analysis performed will include verification of circuit operation, worst case switching delay, worst case switching energy, input capacitances, and output resistance. Design considerations, implementation notes, results, and conclusions will be presented in this report.

# DESIGN

1. Design Choice:

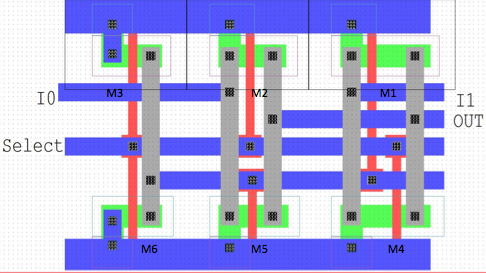
Many configurations of the 2-1 multiplexer have been developed. The performance of different options varies in size, power efficiency, speed, and cost. Our team chose to use CMOS transmission gates with the following considerations:

* Simplicity of design.
* Smallest number of components to assure logic integrity.
* Reasonable performance in speed and power consumption.

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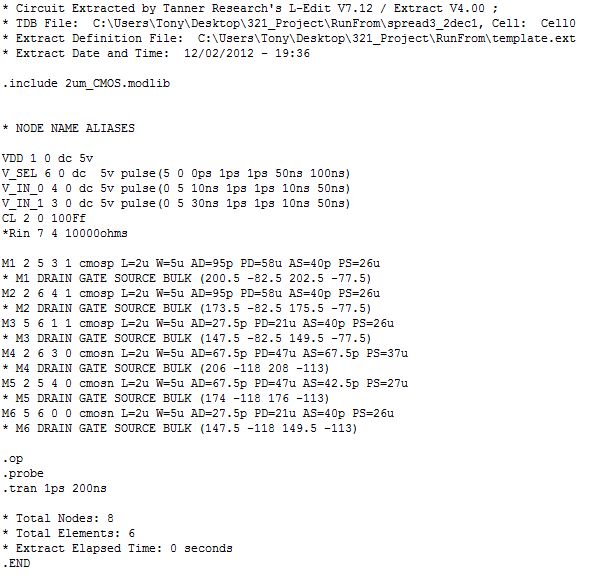
*Figure 1*

1. Layout: (total area = )

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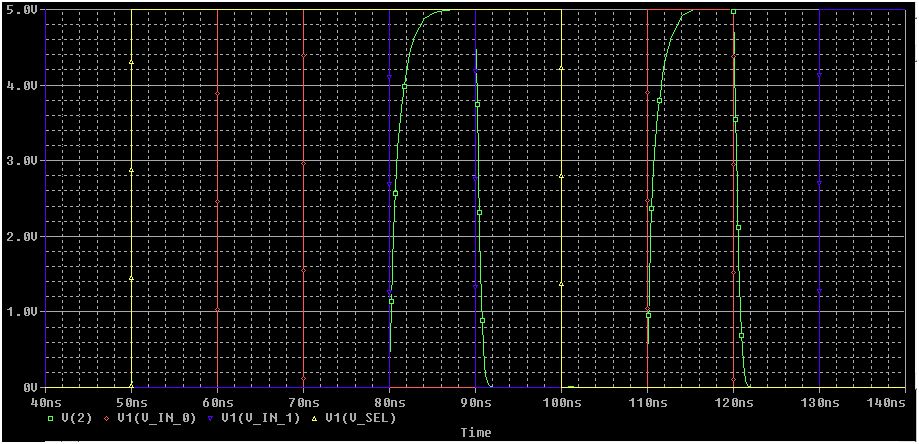
*Figure 2: LEDIT Layout with dimensions.*

Extraction from LEDIT to PSPICE produced a netlist that was edited for node numbering and to add power supply, ground, inputs, and output components. The extracted and adjusted code, listed below, was used to verify integrity of the circuit:



# Implementation / Results

Operation of the circuit was verified in PSPICE by applying pulses to each input in a sequence that allowed each data input to pulse one at a time while the select line was held in each select state for each pair of data pulses. The output followed each data input as expected and the sequence is shown in Figure 3.



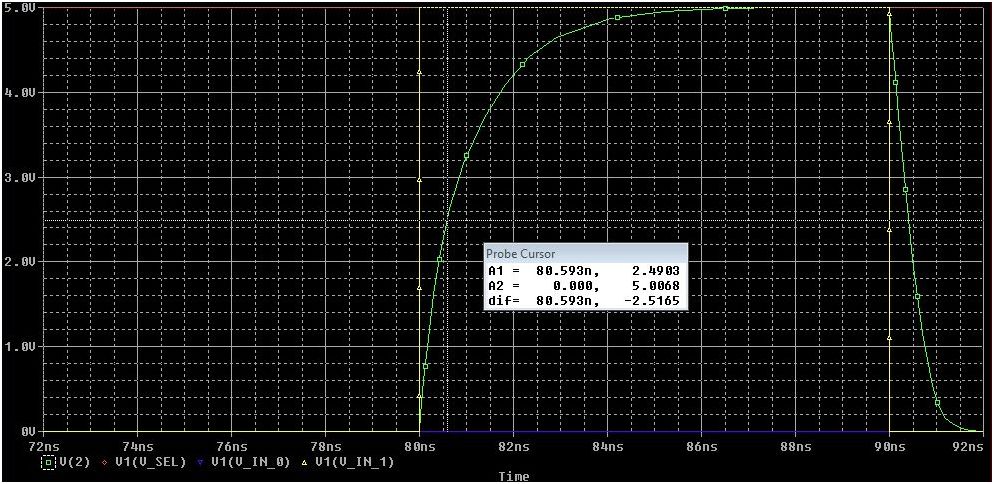
*Figure 3: Verification of operation.*

Transistor states were evaluated in a truth table to determine which state would apply the worst case delay and worst case switching energy. It was determined that two identically sized NMOS transistors on at the same time would carry the lowest drive current and would therefore cause the maximum delay. The truth table and possible worst case states are listed in Table 1.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **SEL** | **I0** | **I1** | **OUT** | **M1** | **M2** | **M3** | **M4** | **M5** | **M6** |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

*Table 1: Transistor states per multiplexer state.*

Worst case output delay was measured in PSPICE and was found to be 593ps. This measurement is shown in Figure 4 below.

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*Figure 4: Worst case delay measurement.*

Capacitances of each input cell were calculated by finding the output delay at the output for a transition of each input then using equation: . Output resistance was calculated using the same equation.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **SEL** | **SEL** | **IO** | **I1** | **Rout** |
| Capacitance | 197.82fF | 138.8fF | 289.85fF |  |
| Resistance |  |  |  | 4.68kΩ |

*Table 2: Cell characterization values.*

|  |  |  |
| --- | --- | --- |
| **Member** | **Task** | **Time** |
| Becker |  |  |
| Mancuso |  |  |
| McConaha |  |  |

*Table 3: Member participation.*

**CONCLUSION**

This project was a good introduction to the basic design process for a digital logic circuit. The 2-1 multiplexer is a very simple circuit that requires no extensive effort to understand and evaluate and the project therefore allowed for extensive focus on operations in LEDIT and PSPICE. Lecture notes and slides allowed for quick development of skills in the use of LEDIT and the application was found to be effective for the purpose of this project. PSPICE skills were improved for the team members due to the redundant effort required to get just the right combination of input pulses and output simulation results. Switching energy proved to be an elusive data that was determined only after a number of hours of research and collaboration with peers. Eventually, the desired results were obtained.

Our work with LEDIT revealed that there are many ways that a circuit can be laid out and different performance enhancements that can be applied, depending on the desired outcome. Testing and analysis of the circuit in PSPICE proved that the circuit operated as intended, and the performance of the circuit seemed to be a good combination of short design and implementation time and reasonable speed and power consumption. It was determined as the project moved forward that there were opportunities to improve size and speed quite easily, however there was insufficient time to implement those improvements at the time of discovery.

In summary, the project provided a sound exposure to transistor logic design and all team members gained valuable experience on sound practices in teamwork, design, and implementation processes.